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Abstract
There are two types of programmable asynchronous circuits in the existing world: the one that is specifically designed for realization of asynchronous circuits on a conventional FPGA board; and a completely re-designed FPGA architecture that fulfills the need of various asynchronous circuits. In recent years, the encountered asynchronous design problems have mainly focused on improvement of routing techniques by adapting dual-rail systems. Although dual-rail possesses the characteristics of quasi-delay insensitive and speed co-dependency among the data signals, but the needed area is two times as much as the single-rail system. Moreover, the delay caused by the probing circuits and non-data-codependent circuits in the dual-rail system are about the same as single-rail, for instance FIFO memories. Therefore, we present a newly programmable asynchronous circuit structure in the thesis.
The programmable asynchronous circuit adopts four-phase protocol and single-rail data bundling in the realization of circuit implementation. We also separate the design into control unit and data computational unit. Since we only need to be extremely positive in achieving a hazard-free condition in the control unit, we could reduce the circuit complexity and area by just focusing on control unit. When we try to implement extended-burst mode asynchronous controller, the use of generalized C-element (gC) is better than any two-level AND-OR gate and Muller C-element combination in the controller design. Therefore, we choose to use gC element in the configurative memory design for the implementation of programmable circuit of the asynchronous circuit controller.
In the data computational unit, we use look-up-table (LUT) as our logic source with a match-delay to control the write-in signal of the register. Since the matched delay is an asymmetric programmable delay element (PDE), it could the configurative memory to slightly lever up signal rising delay time; thus it results in smallest delay time when signal falls. Furthermore, the adapted feature allows reducing of the re-located periods that is wasted in the four-phase protocol, and adds an power-saving mechanism to lower the power dissipation of the PDE.
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